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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/891,885	06/26/2001	Mark T. Ramsbey	F0279	2423

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EXAMINER	
MAGEE, THOMAS J	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 07/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/891,885	RAMSBEY ET AL.	
	Examiner	Art Unit	
	Thomas J. Mag e	2811	

-- Th MAILING DATE of this communication appears on th cover sh et with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9,11-13, and 16-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9,11-13 and 16-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections – 35 U.S.C. 103

3.The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office Action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 9, 11, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Liang et al. (US 6,355,962 B1) in view of Huang (US 5,378,649), Fang (US 6,667,511 B1), and Ojha et al. (US 4,957,873).

5. Regarding Claim 9, Liang et al. disclose a method of forming a flash (non-volatile) memory device, wherein a substrate is provided with memory devices (Col. 1, lines 65 – 67), with one or more insulating regions (20) (Figure 1E) for one or more ESD transistors (Col. 1, lines 62 – 64) formed in the periphery region of the flash memory array (left side, Figure 1E) and poly layers (22A,22B, Figure 1E) over the insulating layers. Liang et al. disclose that after patterning to form ESD and other transistors, spacers are formed (Col. 2, lines 55 – 56) (Figure 1E, 32). Further, Liang et al. do not explicitly disclose that heavy (n+) doping is done with the spacers in place to form source/drain regions (34) (Figure 1E) (Col. 3, lines 7 – 9) for the ESD transistors without masking other transistors in the region. However, Ojha et al. disclose (Col. 2, lines 3 – 6) that a direct write ion beam process can be used for implanting impurities without using a mask. It would have then been obvious to one of ordinary

skill in the art at the time of the invention to use the direct write process of Ohja et al. in Liang et al. to provide can efficient means of implanting the ESD devices without having to mask the other transistors, thereby eliminating one processing step.

Liang et al. do not disclose distinct core and peripheral regions. However, Fang discloses, as part of the prior art (Figure 1a) (Col. 1, lines 21 – 27), that typical non-volatile memory devices comprise one or more high density core regions (11) and a low density peripheral portion on a single substrate. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Fang with Liang et al. to obtain a properly implemented memory device layout.

Liang et al. do not explicitly disclose that word lines in the core region are spaced apart by 1 um or less. Huang discloses (Col. 4, lines 20 – 24) that the polycrystalline silicon word lines used in a non-volatile memory device are spaced at a distance in the range, 0.1 to 0.5 um, consistent with the value recited in the instant application. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Liang et al. and Huang to obtain polysilicon word lines at appropriate spacings to reduce crosstalk and coupling.

6. Regarding Claims 11 and 16, Liang et al. disclose (Col 5, lines 10 – 13) that the source/drain regions are formed by heavy implants of arsenic or phosphorus at an energy of 80 keV to a dose of about 10^(16)/cm(2), consistent with the recitation of claims in the instant application.

7. Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Liang et al. in view of Huang et al. and Fang as applied to Claims 9, 11, and 16, and further in view of Reisinger (US 6,137,718).

8. Regarding Claims 12 and 13, Liang et al. do not explicitly disclose that the flash memory array is a SONOS type structure, but this would have been an easy modification. SONOS cells have been present since the late 1960's. Reisinger discloses (Col. 8, lines 5 12) the formation of MOS transistors with multi-layer dielectrics (51,52,53) capped by a polysilicon layer (6) (See Figure 1) to produce a classical SONOS structure for a non-volatile memory cell. Hence, it would have been obvious to one of ordinary skill in the art at the time of the invention to add Reisinger to Liang et al. to obtain a SONOS structure with improved dielectric properties and increased storage density in the memory circuit (Reisinger, Abstract).

9. Regarding Claims 17 and 18, as discussed above for Claim 9, Liang et al. disclose a method of forming a flash (non-volatile) semiconductor memory device, wherein a substrate is provided with memory devices in a core region with one or more insulating regions (20) (Figure 1E). Liang et al. further disclose (Col. 4, lines 10 – 14) the formation of lightly doped source /drain regions using implants of about 10 ^ (14) ions/cm(2) at an energy of about 80 keV. Liang et al. disclose that after patterning to form ESD and other transistors, spacers are formed (Col. 2, lines 55 – 56) (Figure 1E, 32) from deposited dielectric material. Further, Liang et al. disclose that heavy (n+) doping is done using arsenic or phosphorus at an

energy of 80 keV to a dose of about 10^(16)/cm(2) (Col. 5, lines 10 –13) with the spacers in place to form source/drain regions (34) (Figure 1E) (Col. 3, lines 7 – 9) for the ESD transistors. Liang et al. do not explicitly disclose that heavy (n+) doping is done without masking other transistors in the region. However, Ojha et al. disclose (Col. 2, lines 3 – 6) that a direct write ion beam process can be used for implanting impurities without using a mask. It would have then been obvious to one of ordinary skill in the art at the time of the invention to use the direct write process of Ohja et al. in Liang et al. to provide an efficient means of implanting the ESD devices without having to mask the other transistors, thereby eliminating one processing step.

Response to Arguments

10. Applicant's arguments with respect to claims have been considered but some are moot in view of the new ground(s) of rejection. However, there are a few areas where commentary should be made. In regard to Huang reference, the comments are not germane since there is nothing in the claim language addressing the method of photolithography. Further, the disclosure contained in Fang is a summary of prior art related to memory devices and as such, is readily combined with Liang et al. Commentary related to the Reisinger reference is not germane to the rejection.

Conclusions

11. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to **Thomas Magee**, whose telephone number is **(571) 272**

1658. The Examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM (EST). If attempts to reach the Examiner by telephone are unsuccessful, the examiner's supervisor, **Eddie Lee**, can be reached on **(571) 272-1732.** The fax number for the organization where this application or proceeding is assigned is **(703) 872-9306.**

ORI NADAV
patent examiner

Thomas Magee
March 26, 2004